

What is claimed is:

1. A method for a link layer protocol comprising:
  - 5       reserving a single link unit or a packet for each virtual channel (VC);  
storing a plurality of buffer indexes of a plurality of link units; and  
sharing the remaining link buffers.
2. The method of claim 1 wherein storing the plurality of buffer indexes comprises
  - 10       storing the plurality of buffer indexes in a link buffer or a first in first out memory(FIFO).
3. The method of claim 2 wherein the sharing the remaining link buffers is based at least in part on whether the buffer is used for receiving or transmitting data.
- 15   4. The method of claim 1 wherein sharing the remaining link buffers allows for switching from one list of link units for a first VC is blocked, the link layer by switching from the first VC's link buffer to the second VC's link buffer.
5. An apparatus comprising:
  - 20       a main transmit buffer and a main receiver buffer for each virtual channel (VC);  
a plurality of link buffers to be shared based at least in part on a link buffer or FIFO for each virtual channel; and  
the main receiver and transmit buffers to be sized based at least in part on a round trip

delay.

6. The apparatus of claim 5 wherein the apparatus is a link layer.

7. The apparatus of claim 5 wherein the apparatus facilitates the switch from a first VC's link buffer or FIFO to a second VC's link buffer or FIFO if the first VC's link buffer or FIFO is blocked.

8. A link layer protocol comprising:

a main transmit buffer and a main receiver buffer for each virtual channel (VC);

a plurality of link buffers to be shared based at least in part on a link buffer or FIFO for each virtual channel; and

a sender of a link unit for a VC to indicate whether the link unit utilized a reserved credit or a shared VC buffer; the reserved credit be utilized for a predetermined function if the shared VC buffer is used instead of the reserved credit.

9. The link layer protocol of claim 8 wherein the link layer protocol is utilized as a means of communication to a physical layer.

10. The link layer protocol of claim 8 wherein the link layer protocol facilitates the switch from a first VC's link buffer or FIFO to a second VC's link buffer or FIFO if the first VC's link buffer or FIFO is blocked.

11. The link layer protocol of claim 8 wherein the predetermined function is for a performance critical use.

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12. A system comprising:

at least two processors that are coupled into a point to point network;

10 a main transmit buffer and a main receiver buffer for each virtual channel (VC) for a link layer protocol of the point to point network;

a plurality of link buffers to be shared based at least in part on a link buffer or FIFO for each virtual channel; and

15 a sender of a link unit for a VC to indicate whether the link unit utilized a reserved credit or a shared VC buffer; the reserved credit be utilized for a predetermined function if the shared VC buffer is used instead of the reserved credit.

13. . The system of claim 12 wherein the link layer protocol is utilized as a means of communication to a physical layer.

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14. The system of claim 12 wherein the link layer protocol facilitates the switch from a first VC's link buffer or FIFO to a second VC's link buffer or FIFO if the first VC's link buffer or FIFO is blocked.

15. The system of claim 12 wherein the predetermined function is for a performance critical use.

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16. A system comprising:

at least two processors that are coupled into a point to point network;

a main transmit buffer and a main receiver buffer for each virtual channel (VC) for a link layer protocol of the point to point network;

10 a plurality of link buffers to be shared based at least in part on a link buffer or FIFO for each virtual channel; and

the main receiver and transmit buffers to be sized based at least in part on a round trip delay.

15 17. The system of claim 16 wherein the link layer protocol facilitates the switch from a first VC's link buffer or FIFO to a second VC's link buffer or FIFO if the first VC's link buffer or FIFO is blocked.